The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-6. (Canceled)

7. (Currently Amended) A method of manufacturing a wiring comprising the steps of:

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the first conductive layer, the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width; and

etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

8. (Previously Presented) A method of manufacturing a wiring comprising the steps of:

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer, a second conductive layer with a first width, and a third conductive layer with a second width;

etching the first conductive layer to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a third width, the second conductive layer with the first width, and the third conductive layer with the second width; and

etching the second conductive layer with the first width and the third conductive layer with the second width to form a fourth-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

9. (Currently Amended) A method of manufacturing a wiring comprising the steps of:

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the first conductive layer, the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width;

etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

subjecting the third-shaped conductive layer to a plasma treatment,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

10. (Previously Presented) A method of manufacturing a wiring comprising the steps of:

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer, a second conductive layer with a first width, and a third conductive layer with a second width;

etching the first conductive layer to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a third width, the second conductive layer with the first width, and the third conductive layer with the second width;

etching the second conductive layer with the first width and the third conductive layer with the second width to form a fourth-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

subjecting the fourth-shaped conductive layer to a plasma treatment,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

11. (Original) A method of manufacturing a wiring according to any one of claims 7 to 10 , wherein the first conductive layer comprises at least one selected from the group consisting of W and Mo.

12. (Original) A method of manufacturing a wiring according to any one of claims 7 to 10, wherein the second conductive layer comprises Al.

13. (Original) A method of manufacturing a wiring according to any one of claims 7 to 10, wherein the third conductive layer comprises Ti.

14. (Previously Presented) A method of manufacturing a wiring according to any one of claims 9 and 10, wherein the plasma treatment is conducted in an atmosphere containing at least one of oxygen and H_2O.

15.-20. (Canceled)

21. (Currently Amended) A method of manufacturing a wiring board comprising the steps of:

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the first conductive layer, the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width; and

etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with [[the]] a sixth width,

wherein a cross-section of edges of at least one of the first conductive layer with the fourth width, the second conductive layer with the fifth width, and the third conductive layer with the sixth width has a taper shape.

22. (Previously Presented) A method of manufacturing a wiring board comprising the steps of:

forming a first-shaped conductive layer composed of a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer, a second conductive layer with a first width, and a third conductive layer with a second width;

etching the first conductive layer to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a third width, the second conductive layer with the first width, and the third conductive layer with the second width; and

etching the second conductive layer with the first width and the third conductive layer with the second width to form a fourth-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width,

wherein a cross-section of edges of at least one of the first conductive layer with the fourth width, the second conductive layer with the fifth width, and the third conductive layer with the sixth width has a taper shape.

23. (Currently Amended) A method of manufacturing a wiring board comprising the steps of:

forming a first conductive layer ~~in contact with~~ on an insulating surface;

forming a second conductive layer on the first conductive layer;

forming a third conductive layer on the second conductive layer;

patterning the first, second and third conductive layers by dry etching method to form a conductive layer with a taper portion, wherein fluorine containing gas is used as etching gas for etching at least the first conductive layer; and

subjecting the conductive layer with the taper portion to a plasma treatment.

24. (Currently Amended) A method of manufacturing a wiring board comprising the steps of:

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the first conductive layer, the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of a first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width;

etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with [[the]] a sixth width; and

subjecting the third-shaped conductive layer to a plasma treatment,

wherein a cross-section of edges of at least one of the first conductive layer with the fourth width, the second conductive layer with the fifth width, and the third conductive layer with the sixth width has a taper shape.

25. (Previously Presented) A method of manufacturing a wiring board comprising the steps of:

forming a first-shaped conductive layer composed of a stack of a first conductive layer, a second conductive layer, and a third conductive layer on an insulating surface;

etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer, a second conductive layer with a first width, and a third conductive layer with a second width;

etching the first conductive layer to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a third width, the second conductive layer with the first width, and the third conductive layer with the second width;

etching the second conductive layer with the first width and the third conductive layer with the second width to form a fourth-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

subjecting the fourth-shaped conductive layer to a plasma treatment,

wherein a cross-section of edges of at least one of the first conductive layer with the fourth width, the second conductive layer with the fifth width, and the third conductive layer with the sixth width has a taper shape.

26. (Original) A method of manufacturing a wiring board according to any one of claims 21 to 25, wherein the first conductive layer comprises at least one selected from the group consisting of W and Mo.

27. (Original) A method of manufacturing a wiring board according to any one of claims 21 to 25, wherein the second conductive layer comprises Al.

28. (Original) A method of manufacturing a wiring board according to any one of claims 21 to 25, wherein the third conductive layer comprises Ti.

29. (Previously Presented) A method of manufacturing a wiring board according to any one of claims 23 to 25, wherein the plasma treatment is conducted in an atmosphere containing at least one of oxygen and H_2O.

30.-36. (Canceled)

37. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate;

forming a gate insulating film on the semiconductor layer;

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

etching the first conductive layer, the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width; and

etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

38. (Previously Presented) A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate;

forming a gate insulating film on the semiconductor layer;

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer, a second conductive layer with a first width, and a third conductive layer with a second width;

etching the first conductive layer to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a third width, the second conductive layer with the first width, and the third conductive layer with the second width; and

etching the second conductive layer with the first width and the third conductive layer with the second width to form a fourth-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

39. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate;

forming a gate insulating film on the semiconductor layer;

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

etching the first conductive layer, the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of

the first conductive layer with a first width, a second conductive layer with a second width, and a third conductive layer with a third width;

etching the second conductive layer with the second width and the third conductive layer with the third width to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

subjecting the third-shaped conductive layer to a plasma treatment,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

40. (Previously Presented) A method of manufacturing a semiconductor device comprising the steps of:

forming a semiconductor layer over a substrate;

forming a gate insulating film on the semiconductor layer;

forming a first-shaped conductive layer comprising a lamination of a first conductive layer, a second conductive layer, and a third conductive layer on the gate insulating film;

etching the second conductive layer and the third conductive layer to form a second-shaped conductive layer comprising a lamination of the first conductive layer, a second conductive layer with a first width, and a third conductive layer with a second width;

etching the first conductive layer to form a third-shaped conductive layer comprising a lamination of a first conductive layer with a third width, the second conductive layer with the first width, and the third conductive layer with the second width;

etching the second conductive layer with the first width and the third conductive layer with the second width to form a fourth-shaped conductive layer comprising a

lamination of a first conductive layer with a fourth width, a second conductive layer with a fifth width, and a third conductive layer with a sixth width; and

subjecting the fourth-shaped conductive layer to a plasma treatment,

wherein a cross-section of edges of at least one of the first conductive layer, the second conductive layer, and the third conductive layer has a taper shape.

41. (Original) A method of manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the first conductive layer comprises at least one selected from the group consisting of W and Mo.

42. (Original) A method of manufacturing a semiconductor device according to any one of claims 37 to 40 , wherein the second conductive layer comprises Al.

43. (Original) A method of manufacturing a semiconductor device according to any one of claims 37 to 40 , wherein the third conductive layer comprises Ti.

44. (Previously Presented) A method of manufacturing a semiconductor device according to any one of claims 39 and 40, wherein the plasma treatment is conducted in an atmosphere containing at least one of oxygen and H_2O.

45. (Original) A method of manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the semiconductor device is at least one selected from the group consisting of a liquid crystal display device and a light-emitting device.

46. (Original) A method of manufacturing a semiconductor device according to any one of claims 37 to 40, wherein the semiconductor device is at least one selected from the group consisting of a personal computer, a player using a recording medium, and a display.

47. (Previously Presented) A method of manufacturing a wiring board according to claim 23, wherein a surface of the taper portion of the conductive layer is oxidized by said plasma treatment.

48. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive layer ~~in contact with~~ on an insulating surface;

forming a second conductive layer on the first conductive layer;

forming a third conductive layer on the second conductive layer;

patterning the first, second and third conductive layers by dry etching method to form a conductive layer with a taper portion, wherein fluorine containing gas is used as etching gas for etching at least the first conductive layer; and

subjecting the conductive layer with the taper portion to a plasma treatment.

49. (Previously Presented) A method of manufacturing a semiconductor device according to claim 48, wherein the first conductive layer comprises at least one selected from the group consisting of W and Mo.

50. (Previously Presented) A method of manufacturing a semiconductor device according to claim 48, wherein the second conductive layer comprises Al.

51. (Previously Presented) A method of manufacturing a semiconductor device according to claim 48, wherein the third conductive layer comprises Ti.

52. (Previously Presented) A method of manufacturing a semiconductor device according to claim 48, wherein the plasma treatment is conducted in an atmosphere containing at least one of oxygen and H_2O.

53. (Currently Amended) A method of manufacturing a semiconductor device comprising the steps of:

forming a first conductive layer including any one of tungsten and molybdenum ~~in contact with~~ on an insulating surface;

forming a second conductive layer including aluminum as a main component on the first conductive layer;

forming a third conductive layer including titanium on the second conductive layer;

patterning the first, second and third conductive layers by dry etching method to form a conductive layer with a taper portion, wherein fluorine containing gas is used as etching gas for etching at least the first conductive layer; and

subjecting the conductive layer with the taper portion to a plasma treatment.

54. (Previously Presented) A method of manufacturing a semiconductor device according to claim 53, wherein the plasma treatment is conducted in an atmosphere containing at least one of oxygen and H_2O.

55. (Previously Presented) A method of manufacturing a semiconductor device according to claim 53, wherein a surface of the taper portion of the conductive layer is oxidized by said plasma treatment.